

通信处理器的领导者

超过 **350** 家客户和 **> 5000** 设计范例

超过 **70%** 的市场份额 (来源: 市场调研公司 **Gartner**)

销售量超过 **1** 亿片

PowerQUICC II 的销售量超过 **100** 万片



业内已被证明了的结构设计和无法超越的集成设计

MPC 8540 / MPC 8560

e500 Core

- ◆ 667 MHz up to 1 GHz
- ◆ 32K L1 I-Cache, 32K L1 D-Cache
- ◆ 256K unified L2 cache

DDR Memory Bus

- ◆ 133-166MHz bus (266-333MHz data rates)

2x10/100/1000 MAC

1x10/100 MAC (8540 only)

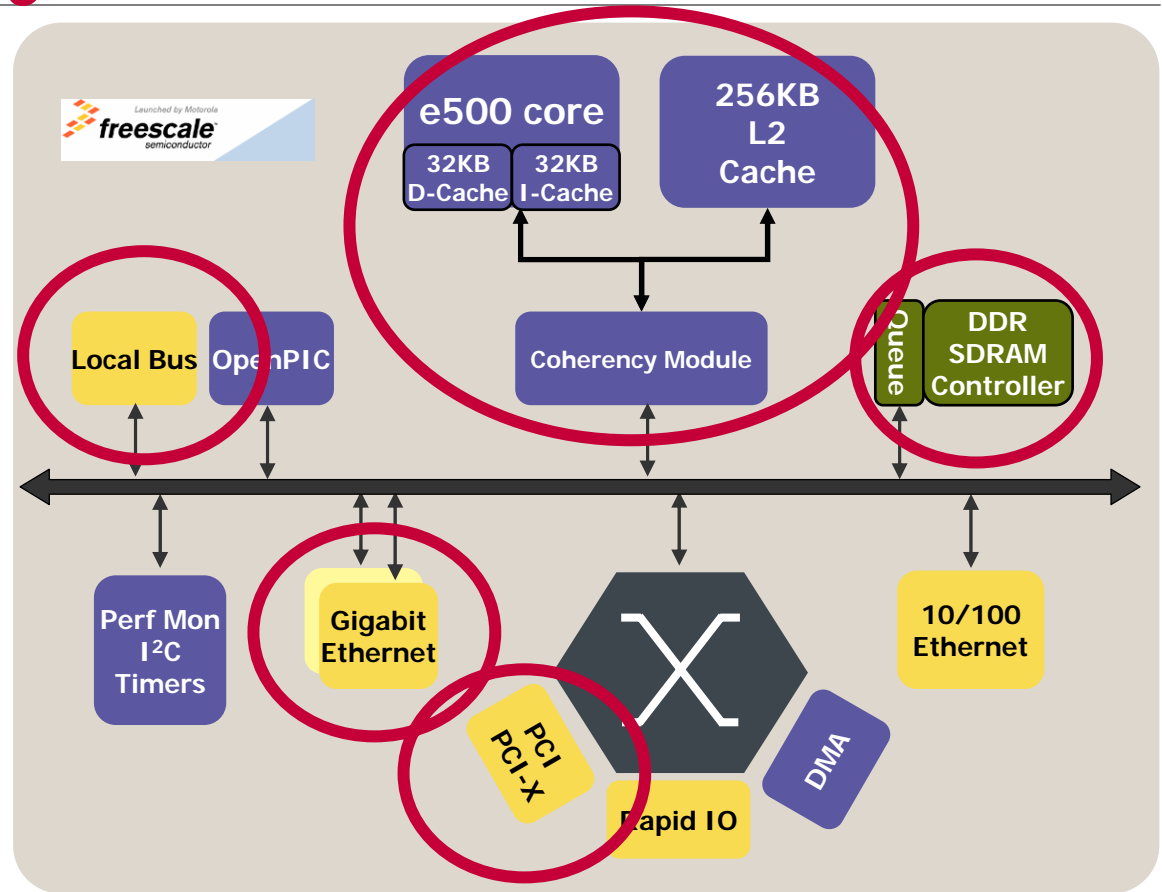
SPI, I2C

Local Bus - (3.3V I/O)

- ◆ 32-bit local bus with memory controller
- ◆ Muxed address/data

PCI-X - (3.3V I/O)

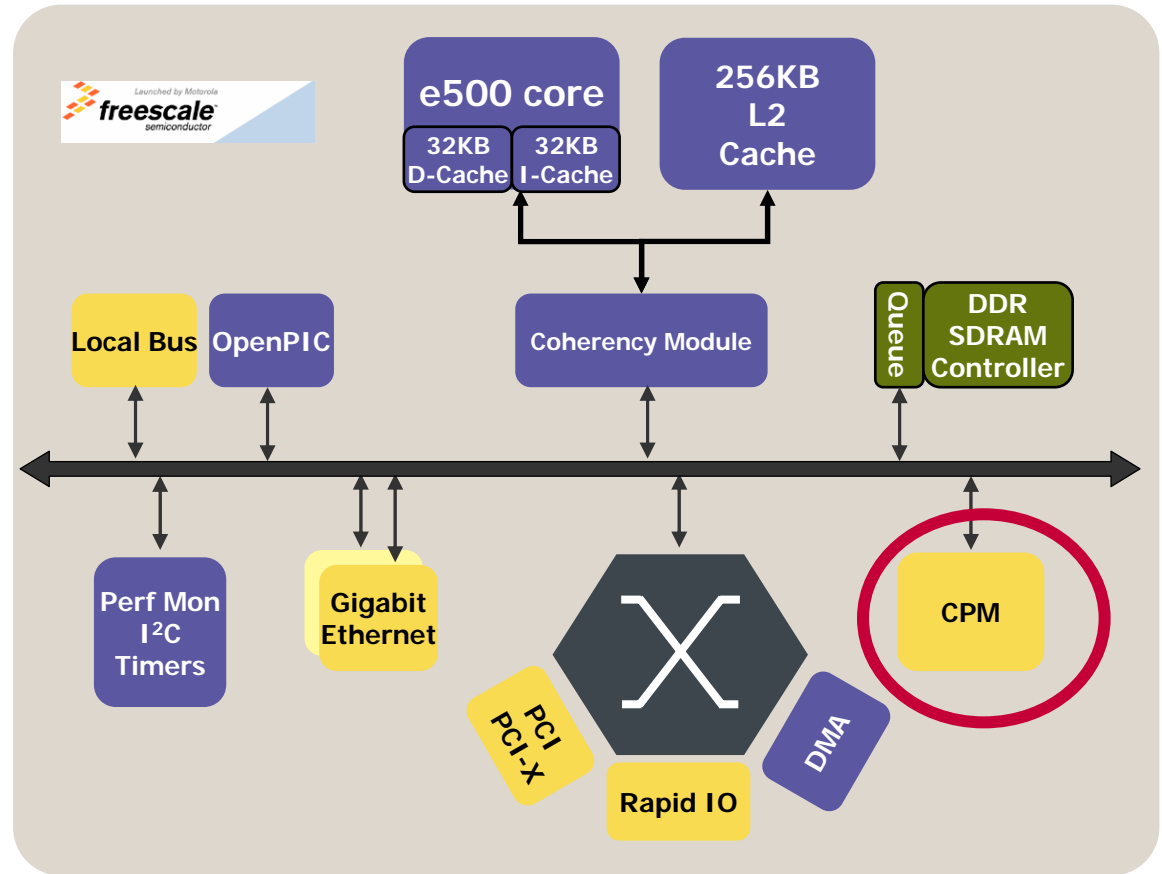
- ◆ 32-/64-bit PCI/PCI-X with int. PCI arbiter



MPC8560 only

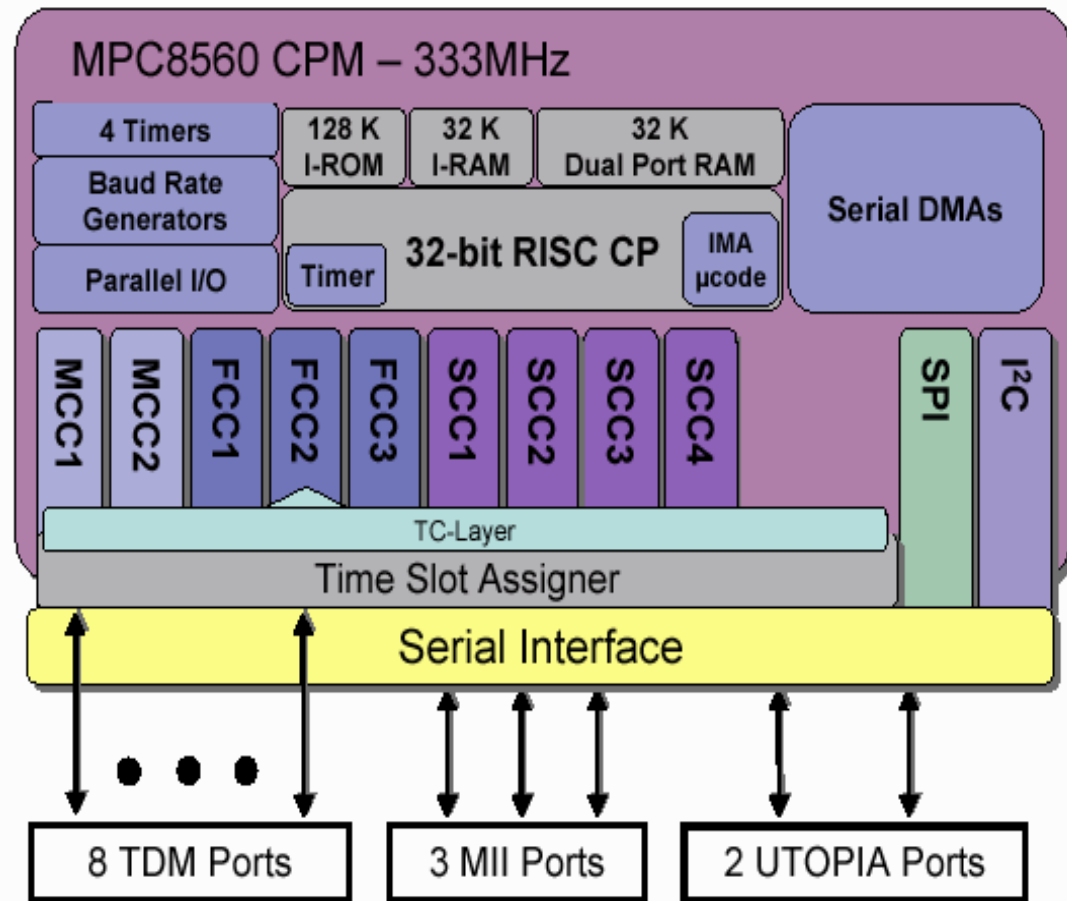
CPM

- ◆ Specialized RISC 333 MHz
- ◆ 3 Fast Communication Channels (FCC):
 - OC-3 ATM, 10/100 Mbit/s
 - Ethernet, E3/T3
 - HDLC/transparent operation
- ◆ 2 Multichannel Communications Controller
 - 256 channels of HDLC/transparent
- ◆ Time Slot assigner channels
 - 8 physical links of up to 16 Mbps or
 - 2 channels of T3/E3
- ◆ 4 Serial Communication Channels (SCC)
 - HDLC, HDLC bus,
 - transparent mode, UART,
 - Bisync, Appletalk/Localtalk
- ◆ 8 channel ATM TC layer



MPC8560's Communications Processor Module (CPM)

- PowerQUICC II like CPM
- High-performance Communication Processor Module (CPM)
 - Independent RISC controller (333 MHz)
 - 32K dual-port RAM for protocol parameters
 - 128K Instruction ROM + 32K Instruction RAM
 - 8 trap registers
- Differences to PQII CPM
 - no IDMA emulation
 - no 10BaseT Ethernet support on SCC
 - no SMC
 - No support of PPC Little-Endian SDMA mode



PQIII platform approach

MPC8540

MPC8560

- PowerQUICC III common platform

- DUART
- DSEC (dual speed 10/100BaseT Ethernet Controller)

- CPM
 - ATM
 - TDM (HDLC, transparent, channelized or unchannelized)
 - other: UART, Bisync, V.35, ...
 - 3 add. 10/100BaseT Ethernet channels
- CPM to local bus path